ABSTRACT

A programmable logic device which incorporates an innovative routing hierarchy consisting of the multiple levels of routing lines, connector tab networks and turn matrices, enables an innovative, space saving floor plan to be utilized in an integrated circuit implementation, and is particularly efficient when an SRAM is used as the configuration bit This floor plan is a scalable block architecture in which each block connector tab networks of a 2 x 2 block grouping is arranged as a mirror image along the adjacent axis relative to each other. Furthermore, the bidirectional input/output lines are provided as the input/output means for each block are oriented only in two directions (instead of the typical north, south, east and west directions) such that the block connector tab networks for adjacent blocks face each other in orientation. This orientation and arrangement permits blocks to share routing resources. In addition, this arrangement enables a 4x4 block grouping to be scalable. The innovative floor plan makes efficient use of die space with little layout dead space as the floor plan provides for a plurality of contiguous memory and passgate arrays (which provide the functionality of the bidirectional switches) with small regions of logic for CFGs and drivers of the block connector tab networks. Therefore, the gaps typically incurred due to a mixture of memory and logic are avoided. Intra-cluster routing lines and bi-directional routing lines are overlayed on different layers of the chip together with memory and passgate arrays to provide connections to higher level routing lines and connections between CFGs in the block.